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» Key

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[Signal Processing Magazine, IEEE](#)
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- ☐ 2. **A VLIW processor with reconfigurable instruction set for embedded applications**
Lodi, A.; Toma, M.; Campi, F.; Cappelli, A.; Canegallo, R.; Guerrieri, R.;
[Solid-State Circuits, IEEE Journal of](#)
Volume 38, Issue 11, Nov. 2003 Page(s):1876 - 1886
Digital Object Identifier 10.1109/JSSC.2003.818292
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1712 KB\)](#) IEEE JNL
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- ☐ 3. **Implementing an OFDM receiver on the RaPID reconfigurable architecture**
Ebeling, C.; Fisher, C.; Guanbin Xing; Manyuan Shen; Hui Liu;
[Computers, IEEE Transactions on](#)
Volume 53, Issue 11, Nov. 2004 Page(s):1436 - 1448
Digital Object Identifier 10.1109/TC.2004.98
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(1352 KB\)](#) IEEE JNL
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- ☐ 4. **A configurable pipelined state machine as a hybrid ASIC and configurable architecture**
Zipf, P.; Stotzler, C.; Glesner, M.;
[VLSI, 2004. Proceedings. IEEE Computer society Annual Symposium on](#)
19-20 Feb. 2004 Page(s):266 - 267
[AbstractPlus](#) | [Full Text: PDF\(214 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- ☐ 5. **A reconfigurable processor architecture and software development environment for embed**
Campi, F.; Cappelli, A.; Guerrieri, R.; Lodi, A.; Toma, M.; La Rosa, A.; Lavagno, L.; Passerone, C.;
[Parallel and Distributed Processing Symposium, 2003. Proceedings. International](#)
22-26 April 2003 Page(s):8 pp.
Digital Object Identifier 10.1109/IPDPS.2003.1213314
[AbstractPlus](#) | [Full Text: PDF\(267 KB\)](#) IEEE CNF

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- 6. A methodical approach for stream-oriented configurable signal processing**
Swanchara, S.; Athanas, P.;
System Sciences, 1999. HICSS-32. Proceedings of the 32nd Annual Hawaii International Conference on System Sciences, 1999. HICSS-32. Proceedings of the 32nd Annual Hawaii International Conference on
Volume Track3, 5-8 Jan. 1999 Page(s):6 pp.
Digital Object Identifier 10.1109/HICSS.1999.772884
[AbstractPlus](#) | Full Text: [PDE\(56 KB\)](#) IEEE CNF
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- 7. A programmable digital neuro-processor design with dynamically reconfigurable pipeline/p**
Young-Jin Jang; Chan-Ho Park; Hyon-Soo Lee;
Parallel and Distributed Systems, 1998. Proceedings., 1998 International Conference on
14-16 Dec. 1998 Page(s):18 - 24
Digital Object Identifier 10.1109/ICPADS.1998.741014
[AbstractPlus](#) | Full Text: [PDE\(1016 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- 8. An ATM application specific integrated processor**
Harasawa, A.; Kaganoi, T.; Kanoh, T.; Nishizaki, H.; Suzuki, M.; Tomizawa, H.; Shindou, T.;
Custom Integrated Circuits Conference, 1997. Proceedings of the IEEE 1997
5-8 May 1997 Page(s):445 - 448
Digital Object Identifier 10.1109/CICC.1997.606663
[AbstractPlus](#) | Full Text: [PDE\(468 KB\)](#) IEEE CNF
[Rights and Permissions](#)
- 9. Streaming processors for next-generation mobile imaging applications**
Chai, S.M.; Chiricescu, S.; Essick, R.; Lucas, B.; May, P.; Moat, K.; Norris, J.M.; Schuette, M.; Lopez,
Communications Magazine, IEEE
Volume 43, Issue 12, Dec. 2005 Page(s):81 - 89
Digital Object Identifier 10.1109/MCOM.2005.1561924
[AbstractPlus](#) | Full Text: [PDE\(276 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- 10. Code size reduction in heterogeneous-connectivity-based DSPs using instruction set exten:**
Biswas, P.; Dutt, N.D.;
Computers, IEEE Transactions on
Volume 54, Issue 10, Oct. 2005 Page(s):1216 - 1226
Digital Object Identifier 10.1109/TC.2005.157
[AbstractPlus](#) | Full Text: [PDE\(1152 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- 11. Resynchronization for multiprocessor DSP systems**
Bhattacharyya, S.S.; Sriram, S.; Lee, E.A.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on (see also Cir
Regular Papers, IEEE Transactions on)
Volume 47, Issue 11, Nov. 2000 Page(s):1597 - 1609
Digital Object Identifier 10.1109/81.895327
[AbstractPlus](#) | [References](#) | Full Text: [PDE\(264 KB\)](#) IEEE JNL
[Rights and Permissions](#)
- 12. Reconfigurable parallel inner product processor architectures**
Rong Lin;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 9, Issue 2, April 2001 Page(s):261 - 272
Digital Object Identifier 10.1109/92.924037
[AbstractPlus](#) | [References](#) | Full Text: [PDE\(340 KB\)](#) IEEE JNL
[Rights and Permissions](#)

- ☐ **13. FPGA prototyping of a RISC processor core for embedded applications**
Gschwind, M.; Salapura, V.; Maurer, D.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 9, Issue 2, April 2001 Page(s):241 - 250
Digital Object Identifier 10.1109/92.924027
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(436 KB) [IEEE JNL](#)
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- ☐ **14. A reconfigurable multilevel parallel texture cache memory with 75-GB/s parallel cache repla**
Se-Jeong Park; Jeong-Su Kim; Ramchan Woo; Se-Joong Lee; Kang-Min Lee; Tae-Hum Yang; Jin-Yoo;
[Solid-State Circuits, IEEE Journal of](#)
Volume 37, Issue 5, May 2002 Page(s):612 - 623
Digital Object Identifier 10.1109/4.997855
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(484 KB) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ **15. Optimization of scannable latches for low energy**
Zyuban, V.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 11, Issue 5, Oct. 2003 Page(s):778 - 788
Digital Object Identifier 10.1109/TVLSI.2003.814322
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(903 KB) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ **16. Programmable stream processors**
Kapasi, U.J.; Rixner, S.; Daffy, W.J.; Khailany, B.; Jung Ho Ahn; Mattson, P.; Owens, J.D.;
[Computer](#)
Volume 36, Issue 8, Aug. 2003 Page(s):54 - 62
Digital Object Identifier 10.1109/MC.2003.1220582
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(564 KB) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ **17. PITIA: an FPGA for throughput-intensive applications**
Singh, A.; Mukherjee, A.; Macchiarulo, L.; Marek-Sadowska, M.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 11, Issue 3, June 2003 Page(s):354 - 363
Digital Object Identifier 10.1109/TVLSI.2003.810780
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(640 KB) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ **18. XDSPCORE: a compiler-based configurable digital signal processor**
Krall, A.; Pryanishnikov, I.; Hirschrott, U.; Panis, C.;
[Micro, IEEE](#)
Volume 24, Issue 4, July-Aug. 2004 Page(s):67 - 78
Digital Object Identifier 10.1109/MM.2004.40
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(184 KB) [IEEE JNL](#)
[Rights and Permissions](#)
- ☐ **19. A method for designing high-radix multiplier-based processing units for multimedia applica**
Guevorkian, D.; Launiainen, A.; Lappalainen, V.; Liuha, P.; Punkka, K.;
[Circuits and Systems for Video Technology, IEEE Transactions on](#)
Volume 15, Issue 5, May 2005 Page(s):716 - 725
Digital Object Identifier 10.1109/TCSVT.2005.846436
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1144 KB) [IEEE JNL](#)
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- ☐ **20. Computation of prime factor DFT and DHT/DCCT algorithms using cyclic and skew-cyclic bi**

IC convolvers

Gudvangen, S.; Holt, A.G.J.;

Circuits, Devices and Systems, IEE Proceedings G

Volume 137, Issue 5, Oct. 1990 Page(s):373 - 389

[AbstractPlus](#) | Full Text: [PDF](#)(976 KB) [IEEE JNL](#)**21. Design and Implementation of an Embedded Microprocessor Compatible with IL Language I Norm IEC 61131-3**

Carrillo, S.; Polo, A.; Esmeral, M.;

Reconfigurable Computing and FPGAs, 2005. ReConFig 2005. International Conference on

28-30 Sept. 2005 Page(s):23 - 23

Digital Object Identifier 10.1109/RECONFIG.2005.14

[AbstractPlus](#) | Full Text: [PDF](#)(232 KB) [IEEE CNF](#)[Rights and Permissions](#)**22. A programmable DSP architecture for wireless communication systems**

Kamalizad, A.; Tabrizi, N.; Bagherzadeh, N.; Hatanaka, A.;

Application-Specific Systems, Architecture Processors, 2005. ASAP 2005. 16th IEEE International

23-25 July 2005 Page(s):231 - 238

Digital Object Identifier 10.1109/ASAP.2005.9

[AbstractPlus](#) | Full Text: [PDF](#)(288 KB) [IEEE CNF](#)[Rights and Permissions](#)**23. An FPGA-Based Floating-Point Jacobi Iterative Solver**

Morris, G.R.; Prasanna, V.K.;

Parallel Architectures, Algorithms and Networks, 2005. ISPAN 2005. Proceedings. 8th International

07-09 Dec. 2005 Page(s):420 - 427

Digital Object Identifier 10.1109/ISPAN.2005.18

[AbstractPlus](#) | Full Text: [PDF](#)(320 KB) [IEEE CNF](#)[Rights and Permissions](#)**24. Functionality Distribution for Parallel Rendering**

Rajagopalan, R.; Goswami, D.; Mudur, S.P.;

Parallel and Distributed Processing Symposium, 2005. Proceedings. 19th IEEE International

04-08 April 2005 Page(s):18 - 18

Digital Object Identifier 10.1109/IPDPS.2005.232

[AbstractPlus](#) | Full Text: [PDF](#)(288 KB) [IEEE CNF](#)[Rights and Permissions](#)**25. Resource sharing and pipelining in coarse-grained reconfigurable architecture for domain-s**

Yoonjin Kim; Kiemb, M.; Park, C.; Jinyong Jung; Kiyoung Choi;

Design, Automation and Test in Europe, 2005. Proceedings

2005 Page(s):12 - 17 Vol. 1

Digital Object Identifier 10.1109/DATE.2005.260

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Chaudhuri, M.; Heinrich, M.;
[Computer Architecture, 2004. Proceedings. 31st Annual International Symposium on](#)
19-23 June 2004 Page(s):124 - 135
Digital Object Identifier 10.1109/ISCA.2004.1310769
[AbstractPlus](#) | Full Text: [PDF](#)(391 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **27. A field programmable bit-serial digital signal processor**
Rahim, S.A.; Turner, L.E.;
[System-on-Chip for Real-Time Applications, 2004. Proceedings. 4th IEEE International Workshop on](#)
19-21 July 2004 Page(s):295 - 298
[AbstractPlus](#) | Full Text: [PDF](#)(263 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **28. High-level optimization of pipeline design**
Campbell, J.P.L.; Day, N.A.;
[High-Level Design Validation and Test Workshop, 2003. Eighth IEEE International](#)
2003 Page(s):43 - 48
Digital Object Identifier 10.1109/HLDVT.2003.1252473
[AbstractPlus](#) | Full Text: [PDF](#)(453 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **29. Picking statistically valid and early simulation points**
Perelman, E.; Hamerly, G.; Calder, B.;
[Parallel Architectures and Compilation Techniques, 2003. PACT 2003. Proceedings. 12th Internat](#)
27 Sept.-1 Oct. 2003 Page(s):244 - 255
Digital Object Identifier 10.1109/PACT.2003.1238020
[AbstractPlus](#) | Full Text: [PDF](#)(356 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **30. Compiler-generated communication for pipelined FPGA applications**
Ziegler, H.E.; Hall, M.W.; Diniz, P.C.;
[Design Automation Conference, 2003. Proceedings](#)
2-6 June 2003 Page(s):610 - 615
[AbstractPlus](#) | Full Text: [PDF](#)(693 KB) IEEE CNF
[Rights and Permissions](#)

- 31. Reconfigurable Viterbi decoder using a new ACS pipelining technique**
Zhu, Y.; Benaissa, M.;
[Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE International Conference on](#)
24-26 June 2003 Page(s):360 - 368
[AbstractPlus](#) | Full Text: [PDF](#)(265 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 32. Unified radix-4 multiplier for GF(p) and GF(2ⁿ)**
Au, L.-S.; Burgess, N.;
[Application-Specific Systems, Architectures, and Processors, 2003. Proceedings. IEEE International Conference on](#)
24-26 June 2003 Page(s):226 - 236
[AbstractPlus](#) | Full Text: [PDF](#)(331 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 33. Branch predictor design and performance estimation for a high performance embedded microprocessor**
Sang-hyuk Lee; Il-kwan Kim; Choi, L.;
[Design Automation Conference, 2003. Proceedings of the ASP-DAC 2003. Asia and South Pacific Design Automation Conference, 2003. Proceedings of the](#)
21-24 Jan. 2003 Page(s):519 - 522
Digital Object Identifier 10.1109/ASPDAC.2003.1195072
[AbstractPlus](#) | Full Text: [PDF](#)(492 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 34. Coarse-grain pipelining on multiple FPGA architectures**
Ziegler, H.; Byoungro So; Hall, M.; Diniz, P.C.;
[Field-Programmable Custom Computing Machines, 2002. Proceedings. 10th Annual IEEE Symposium on](#)
22-24 April 2002 Page(s):77 - 86
Digital Object Identifier 10.1109/FPGA.2002.1106663
[AbstractPlus](#) | Full Text: [PDF](#)(1941 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 35. Automatic verification of in-order execution in microprocessors with fragmented pipelines and functional units**
Mishra, P.; Tomiyama, H.; Dutt, N.; Nicolau, A.;
[Design, Automation and Test in Europe Conference and Exhibition, 2002. Proceedings. DATE 2002](#)
4-8 March 2002 Page(s):36 - 43
Digital Object Identifier 10.1109/DATE.2002.998247
[AbstractPlus](#) | Full Text: [PDF](#)(348 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 36. Architecture exploration of parameterizable EPIC SOC architectures**
Halambe, A.; Cornea, R.; Grun, P.; Dutt, N.; Nicolau, A.;
[Design, Automation and Test in Europe Conference and Exhibition 2000. Proceedings. DATE 2000](#)
27-30 March 2000 Page(s):748
Digital Object Identifier 10.1109/DATE.2000.840881
[AbstractPlus](#) | Full Text: [PDF](#)(20 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 37. Decoupling local variable accesses in a wide-issue superscalar processor**
Sangyeun Cho; Pen-Chung Yew; Gyungho Lee;
[Computer Architecture, 1999. Proceedings of the 26th International Symposium on Computer Architecture, 1999. Proceedings of the](#)
2-4 May 1999 Page(s):100 - 110
Digital Object Identifier 10.1109/ISCA.1999.765943
[AbstractPlus](#) | Full Text: [PDF](#)(796 KB) [IEEE CNF](#)
[Rights and Permissions](#)
- 38. Application of reconfigurable CORDIC architectures**
Mencer, O.; Semeria, L.; Morf, M.; Delosme, J.-M.;
[Signals, Systems & Computers, 1998. Conference Record of the Thirty-Second Asilomar Conference on](#)

Volume 1, 1-4 Nov. 1998 Page(s):182 - 186 vol.1
Digital Object Identifier 10.1109/ACSSC.1998.750850

[AbstractPlus](#) | [Full Text: PDF\(416 KB\)](#) [IEEE CNF](#)
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39. **A scalable FIR filter using 32-bit floating-point complex arithmetic on a configurable component**
Walters, A.; Athanas, P.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium on
15-17 April 1998 Page(s):333 - 334
Digital Object Identifier 10.1109/FPGA.1998.707941
[AbstractPlus](#) | Full Text: [PDF](#)(24 KB) [IEEE CNF](#)
[Rights and Permissions](#)
40. **The systolic array genetic algorithm, an example of systolic arrays as a reconfigurable design**
Bland, I.M.; Megson, G.M.;
FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE Symposium on
15-17 April 1998 Page(s):260 - 261
Digital Object Identifier 10.1109/FPGA.1998.707907
[AbstractPlus](#) | Full Text: [PDF](#)(96 KB) [IEEE CNF](#)
[Rights and Permissions](#)
41. **ASIC design of a microcontroller with power management unit**
Seung-Il Sonh; Hun-Mo Yang; Jong-Ick Lee; Moon-Key Lee;
Semiconductor Conference, 1998. CAS '98 Proceedings, 1998. International
Volume 1, 6-10 Oct. 1998 Page(s):159 - 162 vol.1
Digital Object Identifier 10.1109/SMICND.1998.732324
[AbstractPlus](#) | Full Text: [PDF](#)(352 KB) [IEEE CNF](#)
[Rights and Permissions](#)
42. **Effect of architecture configuration on software reliability and performance estimation**
Mei-Hwa Chen; Mei-Huei Tang; Wen-Li Wang;
Application-Specific Software Engineering Technology, 1998. ASSET '98. Proceedings, 1998. IEEE
26-28 March 1998 Page(s):90 - 95
Digital Object Identifier 10.1109/ASSET.1998.688240
[AbstractPlus](#) | Full Text: [PDF](#)(168 KB) [IEEE CNF](#)
[Rights and Permissions](#)
43. **ATM traffic shaper: ATS**
Diaz, J.C.; Plaza, P.; Crespo, J.;
Design Automation and Test in Europe, 1998. Proceedings
23-26 Feb. 1998 Page(s):96 - 101
Digital Object Identifier 10.1109/DATE.1998.655842
[AbstractPlus](#) | Full Text: [PDF](#)(400 KB) [IEEE CNF](#)
[Rights and Permissions](#)
44. **Two widely-different architectural approaches to computer image generation**
Park, H.W.; Eo, K.S.; Kim, D.L.; Choi, B.K.; Kim, Y.; Alexander, T.;
Visualization, 1991. Visualization '91. Proceedings, IEEE Conference on
22-25 Oct. 1991 Page(s):42 - 49
Digital Object Identifier 10.1109/VISUAL.1991.175776
[AbstractPlus](#) | Full Text: [PDF](#)(688 KB) [IEEE CNF](#)
[Rights and Permissions](#)
45. **Generating synchronous timed descriptions of digital receivers from dynamic data flow system configuration**
Zepter, P.; Grotker, T.;
European Design and Test Conference, 1994. EDAC. The European Conference on Design Automation Test Conference. EUROASIC. The European Event in ASIC Design. Proceedings.
28 Feb.-3 March 1994 Page(s):672

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